Session 12 Overview

Gigabit CDRs and Equalizers

Chair: John T. Stonick, *Synopsys, Hillsboro, OR*

Associate Chair: Jri Lee, *National Taiwan University, Taipei, Taiwan*

Two critical technologies for the design of robust Gb/s communication links are clock and data recovery (CDR) circuits and equalizers. As communication links operate at higher speeds, the symbol intervals are becoming extremely short. At 40Gb/s the entire bit interval is only 25ps! Two papers in this session provide innovative solutions to the problem of operating CDR circuits in CMOS at such speeds. An additional challenge of realizing CDR circuits in shrinking technologies is coping with performance degradation of analog circuit elements. One paper in this session overcomes this challenge with an all-digital CDR. Of course, for a CDR to operate properly; it often requires an equalizer to improve the input signal quality. However, applications and channel degradation vary widely and thus require a broad range of equalizers optimized differently for complexity and power consumption. In this session, 3 equalizer solutions are presented. Finally, while CDR circuits are critical to the performance of most digital communication systems, the session concludes with an interesting study of the power/performance tradeoffs of utilizing transparent mode repeaters in memory interfaces.

The first paper from Seoul U focuses on overcoming the difficulty of realizing CDRs in shrinking process technologies by presenting a purely digital approach to clock and data recovery. The resulting circuit is small in area (0.13mm^2) and achieves 7.2 ps$_{rms}$ jitter when operating at 2.8Gb/s from a sub-1V supply. A key aspect of the design is its 10b DCO which does not utilize any analog circuits.

The pursuit of low-power 40Gb/s CDRs in CMOS is a difficult and compelling problem. In the next 2 papers, two different solutions are presented. In Paper 12.2 from Fujitsu, an oversampling CDR utilizes a 24-phase clock to retime and demultiplex the input into 16 channels. The circuit consumes less than 1W and conforms to the ITU G.8251 jitter tolerance mask. In Paper 12.3 from IBM, a quarter-rate CDR incorporating a phase-programmable clock consumes only 72mW while operating at rates in excess of 40Gb/s. Fabricated in 65nm CMOS technology, it uses no inductors and occupies only 0.03mm^2.

At this point the focus of the session switches from CDRs to the circuits that make them possible to achieve their performance, equalizers. The most challenging channels require DFEs to compensate for ISI impairments without enhancing crosstalk and noise. It is well known that one of the most challenging issues of a DFE is the timing of the loop from the sampler, through the decision circuit and back to the equalizer. In this paper, the concept of loop unrolling or partial response is extended from the first tap to the second tap. An additional innovation is the use of spectrally gated adaptation to prevent the tap drift that can occur during long periods of spectrally non-white data.

A second major hurdle in the deployment of DFEs is their power dissipation. In Paper 12.5 from MIT and IBM, a summing stage based on clocked integrators is adopted to save power. The result is a power consumption of only 9.3mW for 7Gb/s operation. Yes, that is not a typo 9.3mW at 7Gb/s.

In Paper 12.6 from Texas A&M, a 1Gb/s 5-tap T/2 fractionally-spaced transversal equalizer constructed from 3rd-order linear-phase cells is presented. This paper presents an excellent solution to the problem of designing delay cells which have constant group delay and magnitude response over the data bandwidth. An additional key innovation is to improve the bandwidth of the summing circuit by utilizing a transimpedance load. The result is an increase in bandwidth by a factor of 3.6 over a conventional resistive load.

Finally, the session which was initially focused on CDR circuits ends with a twist. Paper 12.7 from Qimonda makes a convincing case for using transparent mode repeaters (no CDR) instead of resampling mode repeaters in point-to-point daisy-chained memory interface operating up to 5.3Gb/s. Operating the repeaters in transparent mode consumes 40% less power and has 80% less latency!

12.1 A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO **8:30 AM**

D-H. Oh, Seoul National University, Seoul, Korea

A 2.8Gb/s all-digital CDR uses a 10b glitch-free DCO which provides a 0.2 to 0.3% frequency tuning step to reduce the quantization effect. The CDR achieves 7.2ps$_{rms}$ jitter at 2.5Gb/s and it operates from a 0.9 to 1.2V supply. The circuit occupies 300×430μm^2 in a 0.13μm CMOS process and dissipates 13.2mW from a 1.2V supply when operating at 2.5Gb/s.

12.2 A 40-to-44Gb/s 3× Oversampling CMOS CDR/1:16 DEMUX **9:00 AM**

N. Nedovic, Fujitsu Laboratories of America, Sunnyvale, CA

A 3× oversampling CDR and 1:16 DEMUX occupies 0.8×1.8mm^2 in a 90nm CMOS process. The chip operates at 40 to 44Gb/s and dissipates 0.91W. Input data is sampled using a 24-phase distributed VCO and a digital CDR recovers 16 bits and a 2.5GHz clock from 48 demultiplexed samples spanning 16UI. Conformance to the ITU G.8251 jitter tolerance mask (BER <10^{-12} with a 2^{31}-1 PRBS source) is demonstrated.

12.3 A 72mW 0.03mm^2 Inductorless 40Gb/s CDR in 65nm SOI CMOS **9:30 AM**

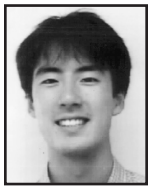
T. Toifl, IBM, Rueschlikon, Switzerland

A quarter-rate CDR circuit is based on a dual-loop approach where sampling phases are generated by a phase-programmable PLL that is controlled by a digital DLL. Implemented in 65nm SOI CMOS, the chip occupies 0.03mm^2 and consumes 1.8mW/Gb/s. Measurements confirm 40Gb/s operation with a BER <10^{-12} at a maximum frequency-offset of 400ppm. The phase relation between data and edge samples can be programmed within ±0.1UI.

12.4 A 7.5Gb/s 10-Tap DFE Receiver with First-Tap Partial Response, Spectrally Gated Adaptation, and 2nd-Order Data-Filtered CDR **10:15 AM**

B. Leibowitz, Rambus, Los Altos, CA

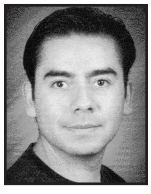
A 7.5Gb/s receiver has a 3-level DFE architecture to satisfy feedback timing requirements for 10 post-cursor taps. The receiver includes a second-order CDR with partial-response transition data filtering as well as a spectrally gated adaptation engine to prevent equalization updates during poor data patterns. The receiver consumes 136mW in a 90nm CMOS process.



12.5 A 7Gb/s 9.3mW 2-Tap Current-Integrating DFE Receiver **10:45 AM**

M. Park, Massachusetts Institute of Technology, Cambridge, MA

A 7Gb/s 2-tap current-integrating DFE implemented in a 90nm CMOS process is presented. Low power dissipation (9.3mW) is achieved by replacing resistively loaded analog current summers with resettable integrators. With 7Gb/s PRBS-7 data, the input sensitivity is 61mV$_{pp\text{-}diff}$, and the DFE equalizes a 16-inch backplane with 45% horizontal eye opening. The DFE core (integrators, latches, clock buffers) occupies 85×65μm^2.



12.6 A CMOS 1Gb/s 5-Tap Transversal Equalizer Based on Inductorless 3rd-Order Delay Cells **11:15 AM**

D. Hernandez-Garduno, Texas A&M University, College Station, TX

The 5-tap FIR structure uses 3rd-order linear-phase cells to implement delays of 500ps for a T/2 fractionally-spaced equalizer. To improve the bandwidth of the summing circuit, the design incorporates a transimpedance load, increasing the bandwidth by a factor of 3.6 over a conventional resistive load. The equalizer consumes 96mW with ±1.5V and occupies 0.26mm^2 in a CMOS 0.35μm process.

12.7 Cascading Techniques for a High-Speed Memory Interface **11:45 AM**

M. Streibl, Qimonda, Munich, Germany

A memory interface operating up to 5.3Gb/s in a 70nm standard DRAM process is presented. The interface uses differential point-to-point signaling in a chain of 6 devices, in transparent- or resample-repeat mode. Transparent-repeat mode measurements at 4.8Gb/s show eye reduction of 8% UI per device due to jitter accumulation. The last device in the repeat chain has an eye opening of 0.5UI at BER<10^{-12}. The transparent-repeat mode consumes 40% less power and has 80% less latency than resample mode.